CLAIMS

What is claimed is:

1. A computer system, comprising:

a processor comprising a cache, a first bus interface and a second bus interface; and

a controller to snoop the cache via the first bus interface during a first mode of operation and to snoop the cache via the second bus interface during a second mode of operation.

2. The computer system of claim 1, further comprising a first bus to couple the first bus interface to the controller, and a second bus to couple the second bus interface to the controller, the first bus being wider than the second bus.

3. The computer system of claim 2, further comprising a main memory and a peripheral device, the peripheral device to request an access of the main memory via the controller.

4. The computer system of claim 1, further comprising a main memory and a peripheral device, the peripheral device to request an access of the main memory via the controller.

5. The computer system of claim 1, wherein the first mode of operation is a high power mode and the second mode of operation is a low power mode.

6. The computer system of claim 5, wherein the first bus interface is to be powered down during the second mode of operation.

7. The computer system of claim 1, further comprising a clock generator, the clock generator to provide a first clock signal to the first bus interface via a clock signal line coupled between the clock generator and the processor, the clock generator to further provide a second clock signal to the second bus interface via a clock signal line coupled between the clock generator and the controller.

8. The computer system of claim 7, wherein the processor further comprises a circuit to provide the first clock signal to the cache during the first mode of operation and to provide the second clock signal to the cache during the second mode of operation.

9. The computer system of claim 8, wherein the processor further comprises a phase-locked loop, and the second clock signal is routed through the phase-locked loop before being provided to the cache during the second mode of operation.

10. The computer system of claim 1, wherein the first bus interface is coupled to the controller via a first bus, the second bus interface is coupled to the

controller via a second bus, and the first bus consumes more power during the first mode of operation than the second bus consumes during the second mode of operation.

11. The computer system of claim 1, wherein the second bus interface is coupled to the controller via a second bus, and the second bus includes a clock signal line for source-synchronous operation, a control line, and a data line.

12. The computer system of claim 11, wherein the first bus interface is coupled to the controller via a first bus, the first bus is a parallel bus, and the second bus is a serial bus having a single data line.

13. A computer system, comprising:

a high power bus;

a low power bus that is narrower than the high power bus and includes a clock signal line for source-synchronous operation;

a processor comprising a cache, a high power bus interface coupled to the high power bus and a low power bus interface coupled to the low power bus; and

a controller to communicate with the processor via the high power bus during a high power mode of operation and to communicate with the processor via the low power bus during a low power mode of operation.

14. The computer system of claim 13, further comprising a main memory and a peripheral device, the peripheral device to request an access of the main memory via the controller.

15. The computer system of claim 13, wherein the high power bus is to be powered down during the low power mode of operation.

16. The computer system of claim 13, wherein the controller is to snoop a memory region of the processor via the high power bus during the high power mode of operation, and the controller is to snoop the memory region via the low power bus during the low power mode of operation.

17. The computer system of claim 16, further comprising a clock generator, the clock generator to provide a clock signal to the memory region via a first clock signal line coupled between the clock generator and the processor during the high power mode of operation, the clock generator to further provide a clock signal to the memory region via the clock signal line of the low power bus during the low power mode of operation.

18. The computer system of claim 13, wherein a clock signal is to be provided via the clock signal line by the controller.

19. The computer system of claim 13, further comprising a power supply to provide a lower voltage supply to the processor during the low power mode of operation than during the high power mode of operation.

20. The computer system of claim 13, wherein the high power bus is a parallel bus that lacks support for source-synchronous operation, and the low power bus is a serial bus having a single data line.

21. An integrated circuit comprising:

a high power bus interface through which a memory region may be snooped during a high power mode of operation; and

a low power bus interface through which the memory region may be snooped during a low power mode of operation.

22. The integrated circuit of claim 21, wherein the high power bus interface is to be powered down during the low power mode of operation.

23. The integrated circuit of claim 21, wherein the high power bus interface supports a first bus, and the low power bus interface supports a second bus that is narrower than the first bus.

24. The integrated circuit of claim 21, wherein the low power bus interface provides for source-synchronous operation and the high power bus interface lacks support for source-synchronous operation.

25. The integrated circuit of claim 21, further comprising a first phase-locked loop (PLL) to provide a clock signal to the memory region during the high power mode of operation, and a second PLL to provide a clock signal to the memory region during the low power mode of operation, the second PLL to receive a clock signal via the low power bus interface.

26. The integrated circuit of claim 21, further comprising a memory bus interface.

27. A method of accessing a cache comprising:

snooping a cache via a high power bus during a high power mode of operation;

transitioning to a low power mode of operation; and

snooping the cache via a low power bus during a low power mode of operation.

28. The method of claim 27, wherein transitioning to a low power mode of operation includes powering down the high power bus.

29. The method of claim 27, wherein snooping the cache via the low power bus includes providing a clock signal to the cache via the low power bus.

30. The method of claim 27, wherein transitioning to the low power mode of operation includes flushing a cache.